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Question Paper Code : 10519

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2025.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 — VLSI DESIGN

(Regulations 2017)

(Common to : Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Sketch a complementary CMOS gate computing $Y(A'B + BC)'$.

2. Write the expression for parasitic delay and logical effort for an N-input NOR gate.

3. Distinguish the dual-rail domino from domino logic.

4. List the sources of power dissipation in CMOS circuits.

5. What is meant by bistability?

6. Define clock-skew and clock-jitter.

7. Draw the circuit diagram of 1-bit binary shifter using MOS transistor.

8. What is the need for sense amplifier in a memory cell?

9. What is the significance of field programmable gate arrays?

10. Write the limitations of IDDQ testing.

PART B — (5 × 13 = 65 marks)

11. (a) Write the layout design rules and draw the diagram for 4 input NOR and 3 input NAND gates.

Or

(b) (i) Explain the DC transfer characteristics of CMOS inverter. (6)

(ii) Estimate the delay of CMOS logic gates as the RC product of the effective driver resistance and the load capacitance. (7)

12. (a) Explain pass transistor logic and show how complementary pass transistor logic and double pass transistor logic applied for 4: 1 MUX. (13)

Or

(b) Sketch a combinational function $W = (XY'+YZ)'$;

(i) Pseudo-nMOS logic (7)

(ii) Cascode voltage switch logic (6)

13. (a) Explain the circuit and working of CMOS implementation of Schmitt trigger.

Or

(b) (i) Describe the concept of pipelining in sequential circuits with suitable example. (7)

(ii) Sketch and explain table sequential circuits based on CMOS logic. (6)

14. (a) (i) Explain the concept of carry look-ahead adder with neat diagram. (9)

(ii) Discuss trade-off between power/speed/area. (4)

Or

(b) Explain in detail the design of low power SRAM memory circuits.

15. (a) Describe FPGA interconnect routing resources with neat diagram.

Or

(b) Explain three main approaches commonly used for Design for Testability (DFT).

PART C — (1 × 15 = 15 marks)

16. (a) Realize a 2-input EX-NOR using static CMOS, transmission gate and dynamic CMOS logic; Also analyze their hardware complexities.

Or

(b) Apply radix-2 encoding to realize a 4-bit signed multiplier for (08)x(-12). For the same multiplier apply radix-8 booth encoding and justify the advantages between radix-4 and radix-8 booth multiplier.